```
   FILE 'REGISTRY' ENTERED AT 09:31:03 ON 08 MAR 2002
                E TUNGSTEN/CN
                E SILICON/CN
                E SILICON/CN
L1            1 S E3
                E POLYSILICON/CN
L2            1 S E3

     FILE 'HCAPLUS' ENTERED AT 09:32:10 ON 08 MAR 2002
L3       386768 S TUNGSTEN OR W OR WOLFRAM
L4       807770 S SILICON OR SI
L5        14848 S POLYSILICON
L6          731 S SILICON ON INSULATOR METAL OXIDE SEMICONDUCTOR OR SOI(W) MOSF
L7       611243 S TRENCH## OR HOLE# OR GROOVE# OR CHANNEL OR EDGE# OR FLUSH OR
L8        51436 S (EPI OR ?EPITAX?)(3N)(LAYER? OR FILM OR FILMS OR COAT####)
L9       314783 S (INSULAT? OR DIELECTRIC OR OXIDE)(3N)(FILM# OR LAYER? OR COAT
L10       77261 S GATE? OR MEMORY()CELL OR LIBRARY()CELL
L11         128 S L6 AND L9
L12       98732 S DRAIN# OR DRIFT# OR (ACTIVE OR DIFFUSION OR SOURCE)(2N)(REGIO
L13          55 S L11 AND L12
L14          38 S L13 AND L7
L15          34 S L14 AND (L5 OR L2 OR METAL?)

     FILE 'REGISTRY' ENTERED AT 09:39:05 ON 08 MAR 2002
                E TUNGSTEN/CN
L16           1 S E3

     FILE 'HCAPLUS' ENTERED AT 09:39:28 ON 08 MAR 2002
L17          32 S L14 AND (L5 OR L2)
L18           6 S L17 AND METAL?
L19           1 S L13 AND L8
L20          48 S L13 AND (L3 OR L1)
L21          12 S L20 AND METAL?
L22           6 S (L19 OR L21) NOT L18
L23         388 S (L16 OR L3) AND (METAL?) AND (L8)
L24           0 S L23 AND L6
L25       43805 S MOSFET OR MOSFETS OR (METAL(W)OXIDE(W)SEMICONDUCTOR) OR NMOS
L26          17 S L25 AND L23
L27          17 S L26 NOT L21
L28          23 S L15 AND L10
L29          19 S L28 NOT (L21 OR L27)
L30        9339 S L16(L)(LAYER? OR FILM OR COAT####)
L31           0 S L6 AND L30
L32         215 S L25 AND L30
L33        1995 S L25 AND (METAL?)(2N)(LAYER? OR FILM OR COAT####)
L34        1112 S L25 AND L8
L35         140 S L32 AND L9
L36          52 S L35 AND L12
L37          23 S L36 AND L7
L38          23 S L37 NOT (L21 OR L27 OR L29)
L39          34 S L14 AND (L5 OR L2 OR METAL? OR L8)
L40          28 S L39 NOT L21
L41           9 S L40 NOT L29
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03/08/2002

L18 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:617442 HCAPLUS
DN 135:173754
TI **SOI MOSFET** devices and fabrication of devices thereof
IN Fung, Ka Hing
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001230423	A2	20010824	JP 2001-78	20010104
	CN 1308378	A	20010815	CN 2000-129498	20001229
PRAI	US 2000-481914	A	20000112		

AB The title devices have buried **metallic** via **holes** each formed directly below body regions each in alignment to gate, wherein the buried **metal** contacts the body region, but does not contact source/**drain**. The structure provides mutual **metal** connections below the devices where .gtoreq.1 mutual connection **layers** contact the Si **insulator film** below the devices via a buried **oxide film**. The arrangement makes possible for connection from the bottom of source/**drain** diffusion layers and from the body regions. The body contacts provides the **SOI MOSFETs** devices with buried **metal** body contacts for compact integration of the circuits.

L18 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:695053 HCAPLUS
DN 131:316300
TI High-temperature characteristics of zone-melting recrystallized silicon-on-insulator MOSFETs
AU Lysenko, V. S.; Rudenko, T. E.; Nazarov, A. N.; Kilchitskaya, V. I.; Rudenko, A. N.; Limanov, A. B.; Colinge, J.-P.
CS Institute of Semiconductor Physics, Kyiv, 252028, Ukraine
SO Fiz. Napivprovidn., Kvantova Optoelektron.. (1998), 1(1), 101-107
CODEN: FNKOF7; ISSN: 1560-8034
PB Natsional'na Akademiya Nauk Ukraini, Institut Fiziki Napivprovidnikiv
DT Journal
LA English
AB The characteristics of enhancement-mode MOS transistors fabricated on zone-melting recrystd. (ZMR) Si-on-**insulator** (SOI) **films** were systematically exptl. studied from 25 to 300.degree.. The main temp.-dependent parameters (the threshold voltage, the **channel** mobility, subthreshold slope, off-state leakage currents) of ZMR **SOI MOSFETs** are described and compared with both theory and SIMOX devices. High carrier mobilities and low off-state leakage currents can be obtained in thin-film ZMR **SOI MOSFETs** at elevated temps. At T = 300.degree., far beyond the operating range of bulk Si devices, the off-state leakage current in ZMR **SOI MOSFETs** with a 0.15 .mu.m-thick Si film was only 0.5 nA/.mu.m (for VD = 3 V), that is 3-4 orders of magnitude lower than typical values in bulk Si devices. The presented results demonstrate that CMOS devices fabricated on sufficiently thin ZMR SOI films are well suited for high-temp. applications.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:409511 HCAPLUS
DN 131:38421
TI Semiconductor device including a **SOI MOSFET** having source and **drain** electrodes comprising a **metal** silicide layer and method of making the same
IN Onishi, Hideaki
PA Nec Corp., Japan
SO Eur. Pat. Appl., 15 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 924773	A1	19990623	EP 1998-123767	19981214
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 11177103	A2	19990702	JP 1997-362498	19971215
	CN 1220496	A	19990623	CN 1998-123350	19981214
	TW 396459	B	20000701	TW 1998-87120779	19981214
PRAI	JP 1997-362498	A	19971215		

AB SOI MOS devices, including MOSFETs, which avoid the narrow line effect are composed of a Si substrate, thin **dielec. film**, and a thin Si film on top. The MOS device has a **channel** region of 1 cond. type and **source** and **drain regions** of a 2nd type and a refractory **metal** silicide adjoining a part of the **source** and **drain regions**. A **polysilicon** layer forms a portion of the Si film between the silicide and the **dielec. film**. A fabrication method involves arsenic ion implantation amorphization of a silicon epitaxial film with subsequent RTA to form the **polysilicon** film.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:96502 HCAPLUS
DN 128:211476
TI Effects of buried **oxide** stress on thin-**film** **silicon**-on-**insulator** **metal**-**oxide**-**semiconductor** field-effect transistor
AU Lee, Jong-Wook; Nam, Myung-Hee; Oh, Jeong-Hee; Yang, Ji-Woon; Lee, Won-Chang; Kim, Hyung-Ki; Oh, Min-Rok; Koh, Yo-Hwan
CS Semiconductor Research Division, Hyundai Electronics Industries Co., Ltd., Ichon-si, Kyoungki-do, 467-860, S. Korea
SO Appl. Phys. Lett. (1998), 72(6), 677-679
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB Thin-**film** Si-on-**insulator** (SOI) device characteristics were studied in terms of stress in the buried oxide interface by both simulation and expt. Bonded SOI wafer with a 400 nm buried oxide and SOI wafer with a 100 nm buried oxide which is made by implanted O were used as a substrate for device fabrication. From the simulation, the 100 nm buried oxide has higher compressive stress than the 400 nm counterpart after the local oxidn. of Si process. With the highly compressive-stressed buried oxide, B atoms may accumulate at the Si side,

esp. at the Si **edge**, under tensile stress so that these accumulated B atoms increase threshold voltage of the **edge channel**. Therefore, there is no hump of the **drain** current in the subthreshold **drain** current-gate-voltage characteristics of thin-film SOI n-**channel metal** -oxide-semiconductor field-effect transistors (MOSFET) with the highly compressed buried oxide.

L18 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:467548 HCAPLUS
DN 123:23152
TI Low-temperature **drain** current characteristics in sub-10-nm-thick SOI nMOSFET's on SIMOX (separation by implanted oxygen) substrates
AU Omura, Yasuhisa; Nagase, Masao
CS NTT LSI Lab., Kanagawa, 243-01, Japan
SO Jpn. J. Appl. Phys., Part 1 (1995), 34(2B), 812-16
CODEN: JAPNDE; ISSN: 0021-4922
DT Journal
LA English
AB This paper describes specific features in low-temp. **drain** current and transconductance characteristics of this silicon-on-insulator n-**channel metal**-oxide-semiconductor field effect transistors (SOI nMOSEFT's) with a sub-10-nm-thick silicon layer and presents some simple anal. based on quantum mechanics. It is suggested that these features originate from the two-dimensional subband system in the thin SOI layer and its local deviation based on the local-deviated silicon layer thickness reflecting the buried **oxide layer** surface morphol. of high-temp.-annealed SIMOX substrates.

L18 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:31485 HCAPLUS
DN 118:31485
TI Thin-film SOI-MOS field-effect transistors and fabrication thereof
IN Matsumoto, Hiroshi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04171766	A2	19920618	JP 1990-299294	19901105

AB The title FET has a small Si region at a 3-corner joining point from a **source region**, a Si interlayer substrate, and an insulative sublayer substrate; where the Si region provides a high concn. of **hole**-electron recombination centers to enhance cancelling of its **hole** concn. The title fabrication involves: (1) forming a component region by component sepn. method on the thin-film SOI substrate; (2) forming a gate **oxide film**; (3) patterning the gate **oxide film**; (4) doping in self-alignment over the patterned gate **oxide film** as its mask to form **source** and **drain regions**; (5) depositing an **insulator** interlayer **film**; (6) annealing for activation; (7) giving a contact **hole**; (8) depositing a **metal** circuit layer; and (9) patterning the circuit layer, wherein the Si region is formed, before or after the formation of the **source** and **drain regions**, by diagonally doping at the 3-corner joining point with an ion possible for the recombination at a level near

the center of its forbidden band width of Si. The **hole**-electron recombination centers provide enhancement for cancellation of a **hole** concn. which otherwise causes deterioration of its withstand voltage in the FET.

03/08/2002

L22 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:136088 HCAPLUS
TI Silicon-on-insulator structure with a body contact
IN Lin, Hongchin; Wong, Shyh-Chyi
PA Windbond Electronics Corp., Taiwan
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6348714	B1	20020219	US 2000-579941	20000526
PRAI	TW 2000-89107354	A	20000419		

AB The present invention relates to a device formed on a silicon-on-insulator (SOI). More particularly, the present invention relates to a MOSFET formed on a SOI with a body contact. A SOI device structure is formed on a SOI substrate having a body contact. The SOI substrate has an **insulating layer** thereon and a Si layer is disposed on the **insulating layer**. A gate is disposed on the Si layer. A **source region** and a **drain** region are resp. disposed within the Si layer beside the gate. A body contact is provided at an interface between the **insulating layer** and the Si layer in which the body contact is preferably located between the **source region** and the gate. The body contact, disposed between the **source region** and the gate can reduce kink effect and body effect, thereby enhancing the performance of device formed on SOI.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:563788 HCAPLUS
DN 135:130818
TI High-frequency **SOI MOSFET** and method of manufacturing the same
IN Bhalla, Anup; Kim, Paul; Korec, Jacek
PA Siliconix Incorporated, USA
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1120835	A2	20010801	EP 2001-101227	20010119
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001244476	A2	20010907	JP 2001-15344	20010124
PRAI	US 2000-491373	A	20000126		

AB A MOSFET is fabricated in a Si-on-insulator (SOI) chip having a relatively thin active **layer** (206) overlying an **oxide** intermediate **layer** (204) and a substrate layer (202). The MOSFET is a lateral device wherein contact is made to the source (212) from the back side of the chip by a conductive plug (246) that extends from the surface of the active layer through the active **layer** and the **oxide layer** (204) into the substrate (202). To improve its performance at high frequencies, the MOSFET may contain a

Si-Ge multilayer (230) structure formed on the active layer and its polysilicon gate (210) may contain an overlying silicide layer (234). The gate oxide may be made thicker at the **drain** end of the gate to protect against the peak elec. field that typically occurs in this region.

L22 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:348066 HCAPLUS
DN 131:95569
TI Buried layer engineering to reduce the **drain**-induced barrier lowering of sub-0.05 .mu.m **SOI-MOSFET**
AU Koh, Risho
CS Silicon Systems Research Laboratories, NEC corporation, Kanagawa, 229-1198, Japan
SO Jpn. J. Appl. Phys., Part 1 (1999), 38(4B), 2294-2299
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB The influence of the buried layer structure on the **drain**-induced barrier lowering (DIBL) was studied for a Si-on-insulator **metal** -oxide-Si field-effect-transistor (**SOI-MOSFET**) by a two-dimensional device simulator. The buried **layer** thickness and the **dielec**. const. of the buried layer are varied systematically. The degrdn. on the threshold voltage can be sepd. into two components. One component originates from the elec. flux via the SOI layer and the other via the buried layer. The buried insulator engineering which controls the thickness and the dielec. const. of the buried layer is effective in reducing the latter component. The gate length limit can be reduced by 23% by the buried air gap structure where the dielec. const. of the buried layer is 1.0.
RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:50928 HCAPLUS
DN 128:161448
TI The influence of the buried oxide defects on the gate oxide reliability and **drain** leakage currents of the **silicon**-on-**insulator metal-oxide-semiconductor** field-effect transistors
AU Iwamatsu, Toshiaki; Ipposhi, Takashi; Yamaguchi, Yasuo; Imai, Yukari; Maegawa, Shigeto; Tsubouchi, Natsuro; Nishimura, Tadashi
CS ULSI Laboratory, Mitsubishi Electric Corporation, Hyogo, 664, Japan
SO Jpn. J. Appl. Phys., Part 1 (1997), 36(12A), 7104-7109
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB The relation between gate oxide and buried oxide (BOX) reliabilities was investigated for several silicon on **insulator** (SOI) **materials**. The yield values of the gate oxide breakdown depend on the BOX leakage currents. The gate leakage currents and BOX leakage currents were obsd. at the same position by optical luminescence. By scanning electron microscope (SEM) observation at the luminescence region in the low-dose sepn. by implanted oxygen (SIMOX) substrate, it was found that the SOI layer had disappeared, and voids appeared in the BOX layer. In addn., Qbd of the gate oxide was low in the capacitor where the BOX leakage currents were obsd. It is thought that the cryst. quality of the SOI layer on the imperfect BOX layer was degraded, causing the gate

leakage currents. Moreover, it was obsd. that the yield value of the **drain** leakage currents of the SOI **metal** -oxide-semiconductor field-effect transistors (MOSFET's) also depended on the BOX leakage currents.

L22 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:466916 HCAPLUS
DN 127:169707
TI An advanced Ge preamorphization salicide technology for ultra-thin-film SOI CMOS devices
AU Hsiao, Tommy C.; Liu, Ping; Woo, Jason C. S.
CS Department of Electrical Engineering, University of California, Los Angeles, CA, 90095, USA
SO IEEE Electron Device Lett. (1997), 18(7), 309-311
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB The authors propose a new approach to implement salicide on thin-**film** silicon-on-**insulator** (SOI) through the amorphization of the source/**drain** (S/D) regions by a germanium implantation. The amorphous film greatly reduces the silicide formation energy and effectively controls the silicide depth. This results in a much lower thermal cycle and increased flexibility in the choice of **metal** thickness. SOI NMOS devices fabricated using this novel salicide technol. have shown substantially reduced S/D resistance as well as good device performance. This technol. is applicable to PMOS **SOI MOSFET**'s as well.

L22 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:421417 HCAPLUS
DN 127:169664
TI Effect of buried oxide thickness in a thin-**film** silicon on **insulator** power **metal**-oxide-semiconductor field-effect transistor
AU Matsumoto, Satoshi; Yachi, Toshiaki
CS NTT Integrated Information and Energy Systems Laboratories, Tokyo, 180, Japan
SO Jpn. J. Appl. Phys., Part 1 (1997), 36(6A), 3438-3442
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB Effect of buried oxide thickness in a thin-**film** Si on **insulator** (SOI) power **metal**-oxide-semiconductor field-effect (MOSFET) transistor is demonstrated. In the thin-film SOI power MOSFETs fabricated on a sepn. by implanted O (SIMOX) substrate, devices with a thin buried oxide showed higher performance than ones with a thick buried oxide. The device with thinner top Si layer operated in a fully depleted mode. The min. specific on-resistance of the fabricated device was 60 m.OMEGA. mm2 at a breakdown voltage of 32 V.

=> D BIB AB 1-5

L27 ANSWER 1 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:123569 HCAPLUS
DN 136:176547
TI Method of making interconnect structure with cobalt silicide diffusion barrier layer
IN Givens, John H.
PA Micron Technology, Inc., USA
SO U.S. Pat. Appl. Publ., 15 pp., Division of U.S. Ser. No. 628,524.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002019127	A1	20020214	US 2001-982191	20011018
PRAI	US 1997-801810	B1	19970214		
	US 1998-198738	B1	19981124		
	US 2000-628524	A3	20000731		

AB Disclosed is a novel method for forming an interconnect structure to provide elec. communication to an isolated junction on a semiconductor substrate assembly. Under the method, an interconnect structure opening extending through an insulating layer to an exposed surface of a junction is provided and a Co layer is deposited in the bottom of the interconnect structure opening. The semiconductor wafer is then annealed to form a Co silicide diffusion barrier layer. A Ti layer may be deposited and used as a diffusion membrane prior to the formation of the Co silicide diffusion barrier layer. The Ti layer also removes native oxide from the bottom of the interconnect structure opening and is stripped off after Co silicide formation. The native oxide may also be cleaned in situ, in which case the Co silicide may be directly formed or it may be formed by depositing a seed layer of Co followed by the co-deposition of Co and Si, an annealing process, and further Co and Si co-deposition. Diffusion barrier liner layer formation and **W metalization** follow. The Co silicide diffusion barrier layer resulting from the novel method is thinner than prior art diffusion barrier **layers**, has better **epitaxial** qualities, and can be sacrificially etched. Cusping and keyholing are reduced and less consumption of Si from the junction occurs. A low resistance diffusion barrier is formed that is resistant to agglomeration.

L27 ANSWER 2 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:582271 HCAPLUS
DN 135:145736
TI CMOS imager with selectively silicided gates
IN Rhodes, Howard E.
PA USA
SO U.S. Pat. Appl. Publ., 18 pp., Division of U.S. Ser. No. 374,990.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001012225	A1	20010809	US 2001-777890	20010207
	US 6333205	B1	20011225	US 1999-374990	19990816
PRAI	US 1999-374990	A3	19990816		

AB The invention relates to an app. and method for selectively providing a

silicide coating over the transistor gates of a CMOS imager to improve the speed of the transistor gates. The method further includes an app. and method for forming a self aligned photo shield over the CMOS imager.

L27 ANSWER 3 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:569739 HCAPLUS
DN 135:130906
TI Method of making **MOSFET** with high dielectric constant gate insulator and minimum overlap capacitance
IN Boyd, Diane Catherine; Hanafi, Hussein Ibrahim; Ieong, Meikei; Natzle, Wesley Charles
PA International Business Machines Corporation, USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6271094	B1	20010807	US 2000-503926	20000214
	JP 2001267565	A2	20010928	JP 2001-17484	20010125
	CN 1309419	A	20010822	CN 2001-102992	20010213
	US 6353249	B1	20020305	US 2001-866239	20010525
	US 2002028555	A1	20020307		
PRAI	US 2000-503926	A	20000214		

AB Methods of fabricating **metal oxide semiconductor** field effect transistor (**MOSFET**) devices having a high dielec. const. (k > 7) gate insulator, low overlap capacitance (0.35 fF/.mu.m or below) and a channel length (sub-lithog., e.g., 0.1 .mu.m or less) that is shorter than the lithog.-defined gate lengths are provided. The methods include a damascene processing step and a chem. oxide removal (COR) step. The COR step produces a large taper on a pad oxide layer which, when combined with a high-k gate insulator, results in low overlap capacitance, sort channel lengths and better device performance as compared to **MOSFET** devices that are formed using conventional complementary **metal oxide semiconductor** (CMOS) technologies.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 4 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:371716 HCAPLUS
DN 134:360268
TI **Metallization** outside protective overcoat for improved capacitors and inductors
IN Erdeljac, John P.; Hutter, Louis Nicholas; Khatibzadeh, M. Ali; Arch, John Kenneth
PA Texas Instruments Incorporated, USA
SO U.S., 30 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6236101	B1	20010522	US 1998-183821	19981030
	US 6284617	B1	20010904	US 2001-776511	20010202
	US 2001019865	A1	20010906		
PRAI	US 1997-64865	P	19971105		

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     US 1998-183821    A3   19981030
AB   A thick layer of Cu is formed on the outside the protective overcoat (PO)
     which protects an integrated circuit, and forms both an inductor and the
     upper electrode of a capacitor.  Placing this layer outside the PO greatly
     reduces parasitic capacitances with the substrate in the devices.
RE.CNT  16     THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27  ANSWER 5 OF 17  HCAPLUS  COPYRIGHT 2002 ACS
AN   2001:355077  HCAPLUS
DN   134:347186
TI   CMP-free disposable gate process
IN   Murtaza, Suhail; Chatterjee, Amitava
PA   Texas Instruments Incorporated, USA
SO   U.S., 14 pp.
     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
     ---------------   ----  --------       ---------------  --------
PI   US 6232188        B1    20010515       US 1998-124854   19980729
PRAI US 1997-54299     P     19970731
AB   A method for forming a MOSFET transistor using a disposable gate
     process which has no need for a chem. mech. polishing step to expose the
     disposable gate after deposition of the field dielec.  The field dielec.
     is deposited nonconformally by HDP-CVD over a disposable gate structure so
     that the disposable gate remains partially exposed.  After deposition, the
     partially exposed disposable gate may then be removed by selective
     isotropic etch.  In the space left by the removal of the disposable gate,
     the gate dielec. may be formed and the gate electrode may be deposited.
     Eliminating the need for exposure of the disposable gate by CMP eliminates
     the problem of polish rate dependence on gate pattern d.
RE.CNT  20     THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT


=> D BIB AB 6-9

L27  ANSWER 6 OF 17  HCAPLUS  COPYRIGHT 2002 ACS
AN   2001:247670  HCAPLUS
DN   134:274470
TI   A nonvolatile memory device with a high work function floating-gate and
     method of fabrication
IN   Mielke, Neal R.; Gill, Manzur
PA   Intel Corporation, USA
SO   PCT Int. Appl., 52 pp.
     CODEN: PIXXD2
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
     ---------------   ----  --------       ---------------  --------
PI   WO 2001024268     A1    20010405       WO 2000-US22784  20000817
         W:  AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN,
             CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR,
             HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT,
             LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU,
             SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN,
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          YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
      RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY,
          DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ,
          CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG
PRAI US 1999-405553    A    19990924
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AB A nonvolatile memory device and its method of fabrication is described. The elec. erasable nonvolatile memory device of the present invention includes a tunnel dielec. formed on a p-type substrate region. A floating-gate having a work function of >4.1 eV is formed on the tunnel dielec. layer. A dielec. is then formed on the floating-gate. a control gate is then formed on the dielec. over the floating-gate.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 7 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:195157 HCAPLUS
DN 134:216057
TI Fabrication of **MOS** transistors and local interconnects using a silicon nitride dummy gate technique
IN Teo, Kok Hin; Chen, Feng; See, Alex; Chan, Lap
PA Chartered Semiconductor Manufacturing, Ltd., Singapore
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6204137	B1	20010320	US 2000-556386	20000424

AB A new method of forming **MOS** transistors was achieved. A pad oxide layer is grown. A Si nitride layer is deposited. Trenches are etched for planned STI. A trench liner is grown inside of the trenches. A trench oxide layer is deposited filling the trenches. The trench oxide layer is polished down to complete the STI. The same Si nitride layer is patterned to form dummy gates. A gate liner layer is deposited. Ions are implanted to form lightly doped drain junctions. Sidewall spacers are formed adjacent to the dummy gate electrodes and the shallow trench isolations. Ions are implanted to form the drain and source junctions. An **epitaxial** Si **layer** is grown overlying the source and drain junctions. A **metal** layer is deposited. The **epitaxial** Si **layer** is converted into silicide to form silicided source and drain contacts. An interlevel dielec. layer is deposited and polished down to the dummy gates. The dummy gates are etched away to form openings for the planned transistor gates. A gate oxide layer is deposited lining the transistor gate openings. A gate electrode layer is deposited to fill the transistor gate openings. The gate electrode layer is patterned to complete the transistor gates.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 8 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:115427 HCAPLUS
DN 134:156465
TI Method for fabricating single crystal materials over CMOS devices by epitaxy
IN Kub, Francis J.; Hobart, Karl D.
PA United States Dept. of the Navy, USA
SO PCT Int. Appl., 51 pp.
CODEN: PIXXD2

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DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.          KIND  DATE          APPLICATION NO.  DATE
     ---------------     ----  --------      ---------------  --------
PI   WO 2001011670       A1    20010215      WO 2000-US17876  20000808
         W:  AU, CA, JP, KR, MX
         RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,
             PT, SE
PRAI US 1999-371782      A     19990810
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AB An aspect of the present invention is a method for making a functional active device (photodetector, laser, LED, optical modulator, optical switch, field effect transistor, **MOSFET**, MODFET, high electron mobility transistor, heterojunction bipolar transistor, resonant tunneling device, Esaki tunneling device etc.) disposed over a complementary **metal oxide semiconductor** (CMOS) device, having the steps: (a) forming an ultrathin compliant layer direct bonded to an oxide layer over said CMOS device; (b) growing an **epitaxial layer** on said ultra-thin compliant layer (c) forming a functional active device in said **epitaxial layer** grown on said **epitaxial layer** that is grown on said ultrathin compliant layer; and (c) interconnecting said functional active device and said CMOS device, wherein said CMOS device is configured as either a readout circuit or a control circuit for said photodetector.

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RE.CNT  9     THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
              ALL CITATIONS AVAILABLE IN THE RE FORMAT
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L27  ANSWER 9 OF 17  HCAPLUS  COPYRIGHT 2002 ACS
AN   1999:8243  HCAPLUS
DN   130:59958
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TI Lateral diffused **MOS** transistor with trench source contact and its fabrication

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IN   Hebert, Francois
PA   Spectrian, USA
SO   PCT Int. Appl., 24 pp.
     CODEN: PIXXD2
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.          KIND  DATE          APPLICATION NO.  DATE
     ---------------     ----  --------      ---------------  --------
PI   WO 9857379          A1    19981217      WO 1998-US11885  19980610
         W:  AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE,
             DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG,
             KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX,
             NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT,
             UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
         RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES,
             FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI,
             CM, GA, GN, ML, MR, NE, SN, TD, TG
     US 5869875          A     19990209      US 1997-872589   19970610
     AU 9878288          A1    19981230      AU 1998-78288    19980610
     EP 988651           A1    20000329      EP 1998-926453   19980610
         R:  DE, FR, GB, IT, NL, SE
     JP 2002504267       T2    20020205      JP 1999-503072   19980610
PRAI US 1997-872589      A     19970610
     WO 1998-US11885     W     19980610
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AB A lateral diffused **MOS** transistor formed in an **epitaxial layer** includes a trench source contact. A method of making the

transistor is also described, including an etch step for the trench.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 10-17

L27 ANSWER 10 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:334182 HCAPLUS
DN 129:61599
TI Semiconductor device and its production method
IN Mitsuwa, Hiroyuki
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10135238	A2	19980522	JP 1996-292448	19961105
	US 6043552	A	20000328	US 1997-964649	19971105
PRAI	JP 1996-292448		19961105		

AB The invention relates to a semiconductor device having an **epitaxial layer** and a conducting layer contg. refractory **metal**, e.g., a bipolar transistor having an epitaxial base or a field effect transistor having an epitaxial source/drain, wherein the refractory **metal** contamination in the **epitaxial layer** due to a heat treatment during the epitaxial growth is prevented by forming a nonmetal conducting layer on the the refractory **metal layer**, and forming a **epitaxial layer** on the nonmetal layer.

L27 ANSWER 11 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:751376 HCAPLUS
DN 126:41326
TI Semiconductor device for **MOS** transistor and its manufacture
IN Nakamura, Yoshitaka; Kobayashi, Nobuyoshi; Kimura, Shinichiro; Myauchi, Akihiro
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08274041	A2	19961018	JP 1995-78582	19950404

AB After forming field oxide films and a gate electrode, Si films are formed selectively on the regions where source/drain diffusion regions will be formed. The Si films may be formed by epitaxy. By the **epitaxy**, the Si **films** are facetted at one edge between the edge of the field oxide film and the Si film. When a (100) Si substrate is used, the facet may be a (111) or (311) plane. Through the facetted Si films, ions are implanted to form source/drain diffusion regions, when source/drain diffusion regions become deep under the facets because the Si film at the facets is thinner than that near the gate electrode. A **metal** silicide film or a high m.p. **metal** film may be self-aligned on the Si film. A device having the facets and deep diffusion regions is

also claimed. The deep diffusion regions prevent the leak-current of the device.

L27 ANSWER 12 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:167977 HCAPLUS
DN 124:247969
TI Semiconductor wafer, semiconductor integrated circuit device, and its manufacture
IN Asakura, Hisao
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 15 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	--------------	----	--------	---------------	--------
PI	JP 07326615	A2	19951212	JP 1994-119958	19940601

AB The wafer comprises a SOI structure of a semiconductor layer on an insulating layer having a buried wiring. The device has a substrate of the SOI structure having a buried wiring working as a semiconductor integrated circuit in an insulating layer. The buried wiring may be a high-m.p. **metal** or low-resistant semiconductor. The manuf. comprises these steps; forming a 1st insulating film on a substrate, forming a buried wiring on the 1st insulating layer, forming a 2nd insulating layer covering the wiring on the 1st layer, (optionally, leveling the surface,) and forming a semiconductor layer on the 2nd insulating layer. The manuf. may contains a patterning process of the wiring so that the relative positions of the device and the wiring might fit, preferably by using IR or electron beam. The manuf. provides good semiconductor device with low wiring d., which makes lay-out design of the wiring easier.

L27 ANSWER 13 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:21523 HCAPLUS
DN 120:21523
TI Integrated circuit devices and their manufacture
IN Shida, Satoshi
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	--------------	----	--------	---------------	--------
PI	JP 05206388	A2	19930813	JP 1992-1148	19920108

AB The devices comprise (a) polycide-structured complementary **MOS** and (b) bipolar transistor having high-concn. buried **layer**, **epitaxial layer**, high-concn. collector lead region, and **metal** silicide formed contacting the lead region formed on semiconductor substrates. The method involves formation of high-concn. buried **layer**, **epitaxial layer**, and field oxide layer on semiconductor substrates in the order; formation of gate oxide; formation of polycryst. Si on the entire surface; removal of polycryst. Si via a mask for formation of collector lead; implantation of high-concn. impurities in collector lead to contact the buried layer; removal of gate oxide and mask on the collector lead region; formation of **metal** silicide on the entire surface; and leaving the polycryst.

Si only on the gate-forming and collector lead regions by patterning.

L27 ANSWER 14 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:439473 HCAPLUS
DN 115:39473
TI Digital capacity transient spectroscopy of deep structure defects in III-V semiconductor structures
AU Korb, Wolfgang
CS Fachbereich Phys., Tech. Univ., Berlin, Fed. Rep. Ger.
SO Report (1989), ETN-90-96057, 145 pp. Avail.: NTIS From: Sci. Tech. Aerosp. Rep. 1990, 28(12), Abstr. No. N90-19890
DT Report
LA German
AB The advantages of Deep Level Transient Spectroscopy (DLTS) methods with digital transients were shown. Different evaluation methods were estd., such as simulated Boxcar processes with many varied time windows and adaptation of multiexponential theory curves at the measurement data with modulation functions. The samples were doped with V, **W**, Ti and Fe. Measurements with n-GaAs-MBE layers showed a Ni-impurity by the growth discontinuity. A defect was found in all MBE layers. With Fe-doped and nondoped p+/n- In GaAs diodes the energetic level of this transient **metal** in InGaAs can be estd. InGaAs-**MOS** structures and contacts with oxide intermediate layers on n minus In P showed a dominating influence of the oxide on the measurements results.

L27 ANSWER 15 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:560824 HCAPLUS
DN 109:160824
TI Deposition of a silicon monolayer on sapphire using an argon fluoride excimer laser for silicon epitaxial growth
AU Ishida, M.; Tanaka, H.; Sawada, K.; Namiki, A.; Nakamura, T.; Ohtake, N.
CS Dep. Electr. Electron. Eng., Toyohashi Univ. Technol., Toyohashi, 440, Japan
SO J. Appl. Phys. (1988), 64(4), 2087-91 CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB Si monolayer deposition on sapphire substrates was investigated by in situ XPS. It involved a direct photolysis of Si2H6 by 193 nm ArF excimer laser light (1-2 **W**/cm2, 70 Hz) at room temp. in a high-vacuum chamber. At first, decompd. Si atoms bound strongly with O atoms on sapphire until the entire sapphire surface was covered, then Si-Si bonds were formed. From the growth mode anal. of the early stage of Si deposition, it can be seen that the growth mode of the deposited layer is a layer-by-layer mode (the Frank-Van der Merwe-type growth). The thickness of the deposited Si layers can be controlled on an at. scale. As these features are suitable for Si-on-sapphire (SOS) **epitaxial** growth with predeposited **layers**, SOS **epitaxial** growth was demonstrated and the SOS films were characterized by replica electron microscopy and fabricating a **metal-oxide-semiconductor** field-effect transistor.

L27 ANSWER 16 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1981:483660 HCAPLUS
DN 95:83660
TI Single and polycrystalline gallium arsenide solar cells using OM-CVD
AU Wang, K. L.; Shin, B. K.; Yeh, Y. C. M.; Stirn, R. J.
CS Jet Propul. Lab., Pasadena, CA, 91103, USA
SO Proc. - Electrochem. Soc. (1979), 79-3(Proc. Int. Conf. Chem. Vap.

Deposition, 7th), 249-60
CODEN: PESODO; ISSN: 0161-6374
DT Journal
LA English
AB High quality GaAs **epi layers** were obtained by a chem. vapor deposition process using organo-**metallic** sources (OM-CVD). Six .mu.-thick GaAs layers grown at 700.degree. on single-crystal substrates showed a Hall mobility as high as 7800 cm2/V-s at 300 K and low residual carrier concn. Polycryst. GaAs films on laser-recrystd. Ge on **W** must be grown at <650.degree. to avoid excessive shunting in solar cells. Large area (1 cm2) AMOS (antireflecting **metal-oxide-semiconductor**) solar cells with 15-16% and 5.7% (air-mass-1) conversion efficiency were obsd. for single-crystal and polycryst. GaAs thin films, resp.

L27 ANSWER 17 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1978:98197 HCAPLUS
DN 88:98197
TI Producing damage in semiconductor bodies
IN Schwuttke, Guenter Helmut; Yank, Kuei-Hsiung; Gorey, Edward Francis
PA International Business Machines Corp., USA
SO Brit., 14 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1483888	A	19770824	GB 1976-10135	19760313

AB Impact sound stressing a semiconductor wafer by placing loose **metal** balls on it and acoustically vibrating it produced microdamage in the wafer in a controlled manner. This treatment improved the generation lifetime and yields of **MOS** capacitors and improved the quality of **epitaxial layers** subsequently grown. E.g., a series of Si wafers was stressed by bouncing 12-mil-diam. **W** balls on the their reverse sides 5 min at 1.38 kHz and 40 **W** to produce 105 Hertzian cracks and damage clusters/cm2. The av. **MOS** yield of capacitors manufd. from 3 P-.ltbbrac.100.rtbbrac. 2 .OMEGA. cm was 91.7% compared with 33.4% for capacitors manufd. from 2 untreated wafers.

03/08/2002

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=> D BIB AB 1-5

L29  ANSWER 1 OF 19  HCAPLUS  COPYRIGHT 2002 ACS
AN   2002:72773  HCAPLUS
DN   136:127697
TI   Method for making SOI MOSFET
IN   Oh, Jeong Hee
PA   Hynix Semiconductor Inc., S. Korea
SO   U.S. Pat. Appl. Publ., 10 pp.
     CODEN: USXXCO
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.       KIND  DATE       APPLICATION NO.   DATE
     ---------------  ----  --------   ---------------   --------
PI   US 2002009859     A1   20020124   US 2001-891193    20010626
     JP 2002033490     A2   20020131   JP 2001-170062    20010605
PRAI KR 2000-37414     A    20000630
AB   Disclosed is a method for making an SOI MOSFET, which
     is capable of improving threshold voltage variations and a parasitic
     bipolar effect generated in the formation of fully depleted (FD) SOI
     semiconductor integrated circuits using a recess channel.  The
     method involves the steps of forming a buried oxide film
     and an active silicon film over a silicon-on-insulator substrate, forming
     a channel at a recess channel, forming dummy spacers
     at opposite side walls of the etched active silicon film, forming a
     gate between the dummy spacers, forming a photoresist film on the
     gate and the active silicon film, forming lightly doped
     drain regions, removing the dummy spacers, forming lightly doped
     ion regions, resp., forming spacers at opposite side walls of the recess
     channel region, resp., removing the photoresist film, forming a
     source region and a drain region,
     forming source/drain electrodes and a gate
     electrode on the resultant structure.

L29  ANSWER 2 OF 19  HCAPLUS  COPYRIGHT 2002 ACS
AN   2001:763499  HCAPLUS
DN   135:297131
TI   SOI semiconductor integrated circuit for eliminating floating body effects
     in SOI MOSFETs and method of fabricating the same
IN   Kim, Young-wug; Kim, Byung-sun; Kang, Hee-sung; Ko, Young-gun; Park,
     Sung-dae; Kim, Min-su; Kim, Kwang-il
PA   Samsung Electronics,co. Ltd, S. Korea
SO   U.S. Pat. Appl. Publ., 33 pp., Cont.-in-part of U.S. Ser. No. 695,341.
     CODEN: USXXCO
DT   Patent
LA   English
FAN.CNT 2
     PATENT NO.       KIND  DATE       APPLICATION NO.   DATE
     ---------------  ----  --------   ---------------   --------
PI   US 2001031518     A1   20011018   US 2001-782116    20010213
PRAI US 1999-161479    P    19991025
     US 2000-695341    A2   20001024
AB   A Si-on-insulator (SOI) integrated circuit and a method of fabricating the
     SOI integrated circuit are provided.  At least 1 isolated transistor
     active region and a body line are formed on an SOI
     substrate.  The transistor active region and the body
     line are surrounded by an isolation layer which is in contact with a
     buried insulating layer of the SOI substrate.  A
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portion of the sidewall of the transistor **active region** is extended to the body line. Thus, the transistor **active region** is elec. connected to the body line through a body extension. The body extension is **covered** with a body **insulating layer**. An insulated **gate** pattern is formed over the transistor **active region**, and 1 end of the **gate** pattern is overlapped with the body **insulating layer**.

L29 ANSWER 3 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:747271 HCAPLUS
DN 135:281691
TI Design and fabrication of a **SOI MOSFET** semiconductor device
IN Adan, Alberto O.
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 21 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1143527	A1	20011010	EP 2001-302968	20010329
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001284591	A2	20011012	JP 2000-102359	20000404
	US 2001028089	A1	20011011	US 2001-822251	20010402
	CN 1316781	A	20011010	CN 2001-117888	20010404
PRAI	JP 2000-102359	A	20000404		

AB A semiconductor device of SOI structure comprises a surface semiconductor layer in a floating state, which is stacked on a buried **insulating film** so as to construct an SOI substrate, **source/ drain regions** of 2nd cond. type which are formed in the surface semiconductor layer, a **channel** region of 1st cond. type between the **source/drain regions** and a **gate** electrode formed on the **channel** region through a **gate insulating film**; in which the surface semiconductor layer has a potential well of the 1st cond. type formed therein at and/or near at least one end of the **channel** region in a **gate** width direction thereof.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 4 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:31776 HCAPLUS
DN 134:109030
TI Lateral thin-**film** silicon-on-**insulator** (SOI) device having a **gate** electrode and a field plate electrode
IN Simpson, Mark; Letavic, Theodore
PA Koninklijke Philips Electronics N.V., Neth.
SO PCT Int. Appl., 15 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 5

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001003201	A1	20010111	WO 2000-EP5956	20000627

W: CN, JP, KR
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE

US 6346451 B1 20020212 US 1999-343912 19990630
EP 1118125 A1 20010725 EP 2000-943905 20000627
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO

PRAI US 1999-343912 A 19990630
US 1997-998048 A2 19971224
WO 2000-EP5956 W 20000627

AB A lateral thin-**film** Si-On-**Insulator** (SOI) device includes a semiconductor substrate, a buried **insulating layer** on the substrate and a lateral transistor device in an SOI **layer** on the buried **insulating layer** and having a **source region** of a 1st cond. type formed in a body region of a 2nd cond. type opposite to that of the 1st. A lateral **drift** region of a 1st cond. type is provided adjacent the body region, and a **drain** region of the 1st cond. type is provided laterally spaced apart from the body region by the **drift** region. A **gate** electrode is provided over a part of the body region in which a **channel** region is formed during operation and extending over a part of the lateral **drift** region adjacent the body region, with the **gate** electrode being at least substantially insulated from the body region and **drift** region by an insulation region. In order to provide improved breakdown voltage characteristics, a **dielec. layer** is provided over at least a part of the insulation region and the **gate** electrode, and a field plate electrode is provided over at least a part of the **dielec. layer** which is in direct contact with the insulation region, with the field plate electrode being connected to an electrode of the lateral transistor device.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 5 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:827079 HCAPLUS
DN 134:79346
TI Simultaneous extraction of the silicon **film** and front **oxide** thicknesses on fully depleted SOI nMOSFETs
AU Nicolett, A. S.; Martino, J. A.; Simoen, E.; Claeys, C.
CS Laboratorio de Sistemas Integraveis, Universidade de Sao Paulo, LSI / PEE / USP, Sao Paulo, SP, 05508-900, Brazil
SO Solid-State Electronics (2000), 44(11), 1961-1969
CODEN: SSELA5; ISSN: 0038-1101
PB Elsevier Science Ltd.
DT Journal
LA English
AB This work presents a new method to ext. the silicon **film** and front **oxide** thickness on fully depleted silicon-on-insulator (SOI) nMOSFETs. The proposed method exploits the influence of the front/back **gate** voltages on the back/front **channel** current regime. To ext. the silicon film thickness, the **drain** current curve is measured as a function of the back **gate** voltage VGB with the front interface inverted. When the back interface condition changes due to the back **gate** voltage, kinks occur in the front **drain** current for specific VGB biases and these are used by the method. Similarly, the back **drain** current as a function of the front **gate** voltage VGF with the back interface inverted shows some kinks at specific VGF, which are used by the method to ext. the front

oxide thickness. MEDICI simulations were used to support the anal., and the method was validated exptl.

RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 6-9

L29 ANSWER 6 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:479683 HCAPLUS
DN 133:66530
TI An analytical model for fully depleted single **gate** SOI MOS transistors including lattice temperature effects
AU Gharabagi, Roobik
CS Department of Electrical Engineering, St Louis University, St Louis, MO, 63156, USA
SO Int. J. Electron. (2000), 87(2), 129-136
CODEN: IJELA2; ISSN: 0020-7217
PB Taylor & Francis Ltd.
DT Journal
LA English
AB An anal. model for fully depleted **SOI MOSFETs** is presented. Major small geometry effects such as carrier velocity satn., mobility degrdn., **channel** length modulation, and **drain** induced barrier lowering are included. Device self-heating due to low thermal cond. of a buried **oxide layer** is included in carrier mobility modeling. Thermal effects are also included in threshold voltage expression. Source, **drain**, and **channel** resistance effects are also included. Modeled results are compared to available measured data and are shown to be in very good agreement.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 7 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:212716 HCAPLUS
DN 132:230290
TI The behavior of narrow-width **SOI MOSFET**'s with MESA isolation
AU Wang, Hongmei; Chan, Mansun; Wang, Yangyuan; Ko, Ping K.
CS Peking University, Beijing, Peop. Rep. China
SO IEEE Trans. Electron Devices (2000), 47(3), 593-600
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Narrow-width effects in thin-**film** silicon-on-**insulator** (**SOI**) **MOSFET**'s with MESA isolation technol. have been studied theor. and exptl. As the **channel** width of the MOSFET is scaled down, the **gate** control of the **channel** potential is enhanced. It leads to the suppression of **drain** current dependence on substrate bias and punch-through effect in narrow-width devices. The variation of threshold voltage with the **channel** width is also studied and is found to have a strong dependence on thickness of silicon film, interface charges in the buried oxide, and **channel** type of **SOI MOSFET**.
RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 8 OF 19 HCAPLUS COPYRIGHT 2002 ACS

AN 1999:653380 HCAPLUS
DN 131:265761
TI Semiconductor devices and method for their fabrication
IN Hwang, Jeong Mo; Son, Jeong Hwan
PA LG Semicon Co., Ltd., S. Korea
SO Ger. Offen., 12 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19900992	A1	19991007	DE 1999-19900992	19990113
	DE 19900992	C2	20010705		
	JP 11297854	A2	19991029	JP 1998-357561	19981216
	JP 3002989	B2	20000124		
	TW 406352	B	20000921	TW 1999-88104413	19990320
	US 6218248	B1	20010417	US 1999-285258	19990402
	US 2001000411	A1	20010426	US 2000-741439	20001221
	US 6337505	B2	20020108		
PRAI	KR 1998-11669	A	19980402		
	US 1999-285258	A3	19990402		

AB In order to prevent floating potentials, a bias potential is applied to a substrate of an **SOI MOSFET**. The semiconductor device has first and second impurity ion- implantation layers of predetd. cond. types in a semiconductor substrate, on which a **covered oxide layer** and silicon **layers** are deposited. First and second transistors are found on the first and second layers with implanted impurity ions and form **drain**- and **source areas** as well as a **gate** area. There are **trenches** between the first and second transistors which extend to the first and second areas that are implanted with impurity ions. Single crystal silicon films are connected with the **drain**- and **source-areas** of the resp. transistors as well as with the first and second impurity ion implanted films and are located on the sides of the **trenches**. Charge carrier emitting electrodes are connected to the first and second impurity-implanted layers resp. on the sides of the resp. transistors,to produce charge carriers that are created in the resp. transistors by impact ionization.

L29 ANSWER 9 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:196456 HCAPLUS
DN 130:203867
TI **SOI-MOSFET** and fabrication process thereof
IN Adan, Alberto O.
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 17 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 902482	A1	19990317	EP 1998-305138	19980629
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 11087719	A2	19990330	JP 1997-241482	19970905
	US 6288425	B1	20010911	US 1998-99107	19980618
PRAI	JP 1997-241482	A	19970905		

AB A **SOI-MOSFET** includes: a substrate; a buried **oxide film** formed on the substrate; a top semiconductor layer formed on the buried **oxide film**, said top semiconductor layer having a portion of a 1st cond. type; a **gate** electrode formed on the top semiconductor **layer** with a **gate oxide film** interposed there between; **source** and **drain regions** of a 2nd cond. type formed in the top semiconductor layer and on both sides of the **gate** electrode;. And an embedded region of the 2nd cond. type which is disposed in the top semiconductor layer and between the **source** and **drain regions** and is sepd. from the **source** and **drain regions** and from an interface between the top semiconductor **layer** and the **gate oxide film**. The embedded region is defined by a tilted implantation of ions of the 1st cond. type, using the **gate** electrode as a mask. The **SOI-MOSFET** has a fully depleted surface **channel** due to the contact potential between said surface **channel** and the embedded region, whereby the Kink effect is prevented.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 10-14

L29 ANSWER 10 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:620113 HCAPLUS
DN 129:296841
TI The dc characteristics of a silicon-on-insulator **metal** -semiconductor field effect transistor
AU Chattopadhyay, P.
CS Department of Electronic Science, University College of Science, Calcutta, 700009, India
SO Semicond. Sci. Technol. (1998), 13(9), 1036-1041
CODEN: SSTEET; ISSN: 0268-1242
PB Institute of Physics Publishing
DT Journal
LA English
AB The dc characteristics of **SOI MOSFETs** were investigated considering the energy distribution of interface states, fixed charges in the **insulating layer** and the effect of back **gate** bias. It is shown that the depletion **layer** arising at the **insulator-channel** interface due to interface states and fixed charges, plays a vital role in fixing the device characteristics. In particular, the role of the above non-idealities on the **drain** current, pinch-off and threshold voltage of the device was investigated. It was found that, when a back **gate** bias is applied, the depletion **layer** width at the **insulator-channel** interface shrinks and the device regains its normal properties overcoming the effects caused by interface states and fixed charges.

L29 ANSWER 11 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:456153 HCAPLUS
DN 129:196451
TI Hot-carrier effects in thin-film deep submicron **SOI/ MOSFET**
AU Cao, Jianmin; Wu, Chuanliang; Shen, Wenzheng; Huang, Chang
CS Xi'an Electronics Techniques Inst., Lintong, 710600, Peop. Rep. China

SO Bandaoti Xuebao (1998), 19(4), 280-286
CODEN: PTTPDZ; ISSN: 0253-4177
PB Kexue Chubanshe
DT Journal
LA Chinese
AB Starting with 2-dimensional simulation of hot-carrier injection current, the authors have discussed the influence of different Si **film** thickness, **gate oxide** thickness and substrate doping on the hot-carrier effects of thin-film deep submicron **SOI/ MOSFET**. Simulation results indicate that for different film thickness, the carrier concn. in front **channel** near the **drain** has different influence on the hot-carrier effects, sometimes the influence is decisive. Previous conflicting reports concerning SOI device hot-carrier effects may result from ignoring the influence of the carrier concn. on the hot-carrier effects. The simulation also indicates that there is a thickness range (60-100 nm), in which the hot-carrier effects is week and insensitive to the thickness. Also, in this range, the hot-carrier effects is independent of **gate** oxide thickness and substrate doping. These is helpful to the design of high reliability thin-film submicron **SOI/ MOSFET**.

L29 ANSWER 12 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:353036 HCAPLUS
DN 129:11616
TI Semiconductor device and its fabrication
IN Maeda, Shigenobu; Yamaguchi, Yasuo; Iwamatsu, Toshiaki
PA Mitsubishi Denki K. K., Japan; Maeda, Shigenobu; Yamaguchi, Yasuo; Iwamatsu, Toshiaki
SO PCT Int. Appl., 76 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9822983	A1	19980528	WO 1996-JP3369	19961115
	W: JP, KR, US				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 948057	A1	19991006	EP 1996-938489	19961115
	R: DE, FR, GB				
	US 2001045601	A1	20011129	US 1998-169903	19981009
PRAI	WO 1996-JP3369	W	19961115		

AB An SOI layer is formed on a Si substrate with a buried **insulating layer** in between. In the SOI layer , **SOI-MOSFET** having a **drain area** and a **source area** which are so formed to define a **channel**-forming area and a **gate** electrode layer facing the **channel** forming area with an **insulating layer** in between is formed. There is provided a field-shield (FS) isolation structure in which an FS plate which faces to the area of the SOI layer near the ends of the **drain** and **source areas** through the **insulating layer** is provided and the **SOI- MOSFET** is elec. isolated from other elements by fixing the potential at the area of the SOI layer facing the plate by imparting a predetd. potential to the FS plate. The **channel** forming area has 2 end sections in the **channel** width direction and a central part between both end sections, and the **channel** length of the area in the end sections of the area is shorter than that in the central

part.

L29 ANSWER 13 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:280563 HCAPLUS
DN 129:74580
TI Short **channel** effects in sub-0.1 .mu.m thin film **SOI-MOSFETs**
AU Rauly, E.; Balestra, F.
CS Laboratoire de Physique des Composants a Semiconducteurs (UMR CNRS/INPG). ENSERG, Grenoble, 38016, Fr.
SO Electron. Lett. (1998), 34(7), 700-701
CODEN: ELLEAK; ISSN: 0013-5194
PB Institution of Electrical Engineers
DT Journal
LA English
AB Short **channel** effects are thoroughly investigated in sub-0.1 .mu.m N **channel SOI-MOSFETs** by using a two-dimensional numerical simulation. **Drain**-induced barrier lowering and charge sharing effects are calcd. as a function of the main device parameters for **gate** lengths down to 0.05 .mu.m. The impact of the silicon **layer**, the **gate oxide** and the buried oxide thicknesses, as well as of the Si film doping, are shown.

L29 ANSWER 14 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:219318 HCAPLUS
DN 128:277841
TI Process for fabricating a fully self-aligned **SOI MOSFET**
IN Venkatesan, Suresh; Poon, Stephen; Lutze, Jeffrey; Ajuria, Sergio
PA Motorola, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5736435	A	19980407	US 1995-497317	19950703

AB A process for fabricating a MOSFET on an SOI substrate includes the formation of an **active region** isolated by field isolation regions and by an **insulating layer**. A recess is formed in the **active region** using a masking layer having an opening therein. A **gate dielec. layer** is formed in the recess and a polycryst. silicon layer is deposited to overlie the masking layer, and to fill the recess. A planarization process is carried out to form a **gate** electrode in the recess, and **source** and **drain regions** are formed in a self-aligned manner to the **gate** electrode. A **channel** region resides intermediate to the **source** and **drain regions** and directly below the **gate** electrode.

=> D BIB AB 15-19

L29 ANSWER 15 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:47783 HCAPLUS
DN 128:161764
TI Insulated **gate** semiconductor devices in prevention of a

substrate floating effect
IN Nishiyama, Akira; Arizumi, Osamu; Yoshimi, Makoto
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10012883	A2	19980116	JP 1996-159996	19960620

AB The title p-**channel** insulative-**gate** devices under subject to a substrate floating effect comprise (1) a 1st n-semiconductor **region** and **source/drain regions** formed on a 1st **insulator film** and (2) a **gate** electrode formed on a 2nd **insulator film** as a **gate insulator** provided on the 1st n-semiconductor region so as to control the current through the 1st semiconductor region. At least one of **source/drain regions** are prepd. by a p-doped 2nd semiconductor region whose forbidden band width is narrower than that of the 1st semiconductor region. The 1st and 2nd semiconductor regions are made from Si and SixGe1-x or SixSn1-x, resp. The 2nd semiconductor region may be made from Si which is subject to stress to a direction towards its lattice const. to be expanded. The device arrangement effectively prevents accumulation of **hole** in the **channel** and consequently avoids the substrate floating effect which is caused by precision fabrication in SOI p-**channel** MOSFETs.

L29 ANSWER 16 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:497338 HCAPLUS
DN 127:227903
TI Short **channel** effects in sub-0.1 .mu.m **SOI-MOSFETs**
AU Rauly, E.; Balestra, F.
CS lab. Phys. Composants Semiconducteurs (UMR-CNRS), ENSERG-INPG, Grenoble, 38016, Fr.
SO Proc. - Electrochem. Soc. (1997), 97-23(Silicon-on-Insulator Technology and Devices), 227-232
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB Short **channel** effects (SCE) were investigated in sub-0.1 .mu.m N **channel SOI-MOSFETs** with two-dimensional numerical simulation. The **Drain**-Induced Barrier Lowering (DIBL) and the charge sharing (CS) effects are calcd. as a function of the main device parameters for **gate** lengths down to 0.05 .mu.m. The thinning of the silicon **layer** and the **gate oxide** leads to a substantial decrease of SCE, whereas the buried oxide has only a slight influence. The impact of the doping of the silicon film is also pointed out.

L29 ANSWER 17 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:393594 HCAPLUS
DN 127:102580
TI 0.18-.mu.m Fully-depleted silicon-on-insulator MOSFET's
AU Cao, Min; Kamins, Ted; Voorde, Paul Vande; Diaz, Carlos; Greene, Wayne
CS ULSI Research Laboratory, Hewlett-Packard Laboratories, Palo Alto, CA,

94304, USA
SO IEEE Electron Device Lett. (1997), 18(6), 251-253
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB High-performance 0.18-.mu.m **gate**-length fully-depleted silicon-on-insulator (FD-**SOI**) **MOSFET**'s were fabricated using 4-nm **gate** oxide, 35-nm thick **channel**, and 80-nm or 150-nm buried **oxide layer**. An elevated source/ **drain** structure was used to provide extra silicon during silicide formation, resulting in low source/**drain** series resistance. Nominal device drive currents of 560 .mu.A/.mu.m and 340 .mu.A/.mu.m were achieved for n-**channel** and p-**channel** devices, resp., at a supply voltage of 1.8 V. Improved short-**channel** performance and reduced self-heating were obsd. for devices with thinner buried **oxide layers**.

L29 ANSWER 18 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:49250 HCAPLUS
DN 126:151624
TI Method of making a body-contacted **SOI MOSFET**
IN Hsu, Ching-hsiang; Liang, Mong-song
PA Taiwan Semiconductor Manufacturing Company Ltd., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5591650	A	19970107	US 1995-488683	19950608
	US 5804858	A	19980908	US 1996-721667	19960927
PRAI	US 1995-488683		19950608		

AB A new method of forming a Si-on-insulator device having a body node contact is described. **Active areas** are isolated from each other within a Si-on-**insulator layer**. Adjacent **active areas** are doped with dopants of opposite polarities to form .gtoreq.1 n-**channel active area** and .gtoreq.1 p-**channel active area**. **Gate** electrodes are formed over each **active area**. The area directly underlying the **gate** electrode and extending downward to the **insulator layer** comprises the body node. Lightly doped areas are formed beneath the spacers on the sidewalls of the **gate** electrodes. First ions are implanted into the **active areas** not covered by a mask, whereby **source** and **drain regions** are formed in the .gtoreq.1 n-**channel active area** and whereby a p-**channel** body contact region is formed within the .gtoreq.1 p-**channel active area** where the p-**channel** body contact region contacts the p-**channel** body node. Second ions are implanted into the **active areas** not covered by a mask, whereby **source** and **drain regions** are formed in the .gtoreq.1 p-**channel active area** and whereby an n-**channel** body contact region is formed within the .gtoreq.1 n-**channel active area** where the n-**channel** body contact region contacts the n-**channel** body node. The semiconductor substrate is annealed to complete formation of

the Si-on-insulator device having a body node contact in the manuf. of an integrated circuit.

L29 ANSWER 19 OF 19 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:764013 HCAPLUS
DN 126:68318
TI Double-charge-sheet model for thin silicon-on-**insulator films**
AU Arnold, Emil
CS Philips Lab., Philips Electronics North America Corp., Briarcliff Manor, NY, 10510, USA
SO IEEE Trans. Electron Devices (1996), 43(12), 2153-2163
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A simple algorithm is proposed that facilitates the calcn. of surface potentials and charge densities at the front and back interfaces in thin Si-on-**insulator** (SOI) **layers** by decoupling of the potentials and charges at the two interfaces. An expression relating the front surface potential and inversion charge to the front and back **gates** biases is derived and compared with a numerical soln. of Poisson's equation. The charge-sheet model agrees well with the simulation results over the front-surface bias range from weak to heavy inversion and with the back Si surface biased into accumulation, depletion, and inversion. The results are reasonably accurate for all doping densities of common interest and for SOI film thicknesses .gtorsim.20 nm. An extension of the model to a nonequil. system was used to derive an expression for the **drain** current in a fully-depleted **SOI MOSFET**. Other applications of the model include a closed-form anal. soln. for the threshold voltage and a calcn. of the interface-state trapped charge.

=> D BIB AB 1-9

L41 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:613896 HCAPLUS
DN 135:311543
TI Advanced SOI p-MOSFETs with strained-Si **channel** on SiGe-on-insulator substrate fabricated by SIMOX technology
AU Mizuno, Tomohisa; Sugiyama, Naoharu; Kurobe, Atsushi; Takagi, Shin-ichi
CS Advanced LSI Technology Laboratory, Toshiba Corporation, Yokohama, 235-8522, Japan
SO IEEE Trans. Electron Devices (2001), 48(8), 1612-1618
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB We have newly developed an advanced SOI p-MOSFET with strained-Si **channel** on insulator (strained-SOI) structure fabricated by SIMOX (sepn.-by-implanted-oxygen) technol. The characteristics of this strained-SOI substrate and elec. properties of strained-**SOI MOSFETs** have been exptl. studied. Using strained-Si/relaxed-SiGe epitaxy technol. and usual SIMOX process, we have successfully formed the layered structure of fully-strained-Si (20 nm)/fully-relaxed-SiGe film (290 nm) on uniform buried **oxide layer** (85 nm) inside SiGe layer. Good **drain** current characteristics have been obtained in strained-**SOI MOSFETs**. It is found that the **hole** mobility is enhanced in strained-SOI p-MOSFETs, compared to the universal **hole** mobility in an inversion layer and the mobility of control SOI p-MOSFETs. The enhancement of the drive current has been kept const. down to 0.3 .mu.m of the effective **channel** length.
RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:246895 HCAPLUS
DN 134:274461
TI Manufacture of **SOI-MOSFETs**
IN Tsuchiaki, Masakatsu
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001094111	A2	20010406	JP 1999-269108	19990922

AB The Si layers in SOI wafers are thinned as well as the **insulator films** under **channel regions**, **source/ drain regions** are formed such that they reach the Si substrates below the **insulator films**, and 2nd **channels** are formed at the interface of the **insulator films** and the substrates, where the **insulator films** are made of **oxides** resistive to HF.

L41 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:55361 HCAPLUS
DN 132:86405
TI Monte Carlo simulation of conductance characteristics in **SOI-**

MOSFET
AU Araya, S.; Yamasaki, K.; Ueno, H.; Mori, N.; Hamaguchi, C.; Perron, L. M.; Lacaita, A. L.
CS Department of Electronic Engineering, Osaka University, Suita City, 565-0871, Japan
SO Physica B (Amsterdam) (1999), 272(1-4), 565-567
CODEN: PHYBE3; ISSN: 0921-4526
PB Elsevier Science B.V.
DT Journal
LA English
AB Front- and back-**channel drain**-conductance characteristics of **SOI-MOSFETs** are calcd. by performing a Monte Carlo simulation, and the calcd. results are compared with published exptl. results in order to ext. the roughness parameters of the two interfaces. Effect of image charge in **oxide layers** in SOI structures is also discussed.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:670798 HCAPLUS
DN 131:305644
TI Exploration of velocity overshoot in a high-performance deep sub-0.1-.mu.m **SOI MOSFET** with asymmetric **channel** profile
AU Cheng, Baohong; Rao, V. Ramgopal; Woo, Jason C. S.
CS APRDL, Austin, TX, 78721, USA
SO IEEE Electron Device Lett. (1999), 20(10), 538-540
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB The electron velocity overshoot phenomenon in the inversion layer is exptl. investigated using a novel thin-**film** silicon-on-**insulator** (SOI) test structure with **channel** lengths down to 0.08 .mu.m. The uniformity of the carrier d. and tangential field is realized by employing a lateral asym. **channel** profile. The electron **drift** velocity obsd. in this work is 9.5 .times. 106 cm/s for a device with effective **channel** length 0.08 .mu.m at 300 K. The upward trend in electron velocity can be clearly noticed for decreasing **channel** lengths.
RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:204850 HCAPLUS
DN 130:304589
TI Effects of buried oxide on electrical performance of thin-**film silicon**-on-**insulator metal-oxide-semiconductor** field-effect transistor
AU Lee, Jong-Wook; Oh, Min-Rok; Koh, Yo-Hwan
CS Semiconductor Research Division, Hyundai Electronics Industries Co., Ltd., Ichon-si, Kyoungki-do, 467-701, S. Korea
SO J. Appl. Phys. (1999), 85(7), 3912-3915
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB Local oxidn. of silicon-isolated thin-**film** silicon-on-**insulator** (SOI) device characteristics have been investigated in

terms of stress in the buried-oxide interface by both simulation and expt. A bonded SOI wafer with a 400 nm buried oxide and a sepn. by implanted oxygen SOI wafer with a 100 nm buried oxide are used for device fabrication. In the 100 nm buried-oxide case, boron atoms are accumulated at the silicon side in the interface between the silicon **film** and **oxide** (i.e., including the buried oxide and field oxide) due to a highly stressed oxide so that the increased boron concn. increases the threshold voltage of the **edge channel**. Therefore, it is found that there is no **drain** current hump in the subthreshold region of thin-film SOI n-**channel metal** -oxide-semiconductor field-effect transistors with 100 nm buried oxide. From the simulation, it is demonstrated that the 100 nm buried oxide has higher compressive stress than the 400 nm counterpart after the local oxidn. of silicon process.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:183745 HCAPLUS
DN 126:286064
TI Reduction of the reverse short **channel** effect in thick **SOI MOSFET**'s
AU Tsoukalas, D.; Tsamis, C.; Kouvatsos, D. N.; Revva, P.; Tsoi, E.
CS Institute of Microelectronics, NCSR "Demokritos", Aghia Paraskevi, 15310, Greece
SO IEEE Electron Device Lett. (1997), 18(3), 90-92
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB We show that the reverse short **channel** effect (RSCE) is reduced in NMOS devices made in thick silicon-on-**insulator** (SOI) **material**. The redn. of the RSCE depends on the thickness of the Si overlayer. It is found that the thinner the Si film, the less the threshold voltage roll-on. The exptl. findings are explained by a decrease of the lateral distribution of silicon interstitials generated at the source and **drain** (S/D) region and are related with their high recombination velocity at the buried oxide. This method can be used to sep. test the influence of S/D point defects on the RSCE from other different hypotheses reported in the literature. Coupled process-device simulation reveals that the method is very sensitive to fundamental point defect properties.

L41 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:433196 HCAPLUS
DN 125:101495
TI Suppressing the parasitic bipolar action of ultra-thin **SOI MOSFET**'s using back-side-bias-temperature treatment
AU Koizumi, Hiroshi; Shimaya, Masakazu; Tsuchiya, Toshiaki
CS NTT LSI Laboratories, Atsugi, 243-01, Japan
SO Annu. Proc. - Reliab. Phys. [Symp.] (1996), 34th, 27-32
CODEN: ARLPBI; ISSN: 0099-9512
DT Journal
LA English
AB A new suppression method for parasitic bipolar action is presented for fully depleted surface-**channel** nMOSFET's on SOI by using the back-side-bias-temp. (BSBT) treatment technique. This method improves subthreshold characteristics, source-**drain** breakdown voltage, and hot-carrier instability without degrading device characteristics.

BSBT treatment can suppress the parasitic bipolar action regardless of stress bias polarity. BSBT damage to the back-side interface between buried **oxide** and active Si **layer** was studied using several methods. The suppression mechanism proposed is the generation of fixed charges and interface traps at the back-side interface.

L41 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:250913 HCAPLUS
DN 124:329453
TI Comparison of standard and low-dose separation-by-implanted-oxygen substrates for 0.1-.mu.m **SOI MOSFET** applications
AU Joachim, Hans-Oliver; Yamaguchi, Yasuo; Fujino, Takeshi; Kato, Takaaki; Inoue, Yasuo; Hirao, Tadashi
CS ULSI Lab., Mitsubishi Elec. Corp., Hyogo, 664, Japan
SO Jpn. J. Appl. Phys., Part 1 (1996), 35(2B), 983-7
CODEN: JAPNDE; ISSN: 0021-4922
DT Journal
LA English
AB The influence of buried oxide thickness on short-**channel** effects in silicon-on-insulator MOSFET transistors (**SOI MOSFET**'s) is investigated. It is shown by anal. modeling and numerical simulation that, although a thin buried oxide helps to reduce the charge-sharing component of source and **drain** elec. fields through the **oxide layers**, substrate depletion underneath the thin buried oxide counteracts the oxide thinning. Although this effect is desired below the **source** and **drain regions** to maintain the SOI inherent low junction capacitances, it is detrimental to short-**channel**-effect suppression. The calcd. results are exptl. confirmed on 0.1-.mu.m **SOI MOSFET**'s fabricated on both std. and low-dose sepn.-by-implanted-oxygen (SIMOX) substrates. A new structure for 0.15-.mu.m **SOI MOSFET** applications on a thin buried oxide substrate is proposed in which substrate depletion below the **channel**-forming region can be suppressed locally using self-aligned deep ion implantation.

L41 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:377329 HCAPLUS
DN 122:303864
TI Investigation of self-heating effects in submicron **SOI MOSFETs**
AU Dallmann, Douglas A.; Shenai, Krishna
CS Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI, 53706, USA
SO Proc. SPIE-Int. Soc. Opt. Eng. (1994), 2369(27th International Symposium on Microelectronics, 1994), 625-30
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB The presence of a buried **oxide layer** in Si causes enhanced self-heating in Si-On-Insulator (SOI) n-**channel** MOSFETs. The self-heating becomes more pronounced as device dimensions are reduced into the submicron regime. Two-dimensional numerical simulations were used to show that self-heating manifests itself as degraded drive current due to mobility redn. The heat flow equation was consistently solved with the classical semiconductor equations to study the effect of power dissipation on carrier transport. The simulated temp. increase in the **channel** region is in close agreement with recently measured data. Numerical simulation results also demonstrated accelerated turn-on of the parasitic bipolar transistor due to

self-heating. Simulation results were used to identify important scaling constraints caused by the bipolar transistor turn-on effect in SOI CMOS ULSI. In the deep submicron regime, SOI devices exhibited a neg. differential resistance due to increased self-heating with **drain** bias voltage. Detailed comparison with bulk devices suggested significant redn. in the **drain**-source avalanche breakdown voltage due to increased carrier injection at the source-body junction. These results place important limits on the max. supply voltage that can be applied.

=> D BIB AB 1-5

L38 ANSWER 1 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:747066 HCAPLUS
DN 135:297034
TI Semiconductor device and procedure for its production.
IN Okumara, Yoshinori; Yamashita, Tomohiro
PA Mitsubishi Denki K.K., Japan
SO Ger. Offen., 122 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 10056272	A1	20011011	DE 2000-10056272	20001114
	JP 2001284467	A2	20011012	JP 2000-93260	20000330
PRAI	JP 2000-93260	A	20000330		

AB The penetration of a gate **insulating film** and the increase of the surface resistance in a gate electrode in a CMOS logic device are prevented in this invention, and the rising surface of a logic gate arrangement in the CMOS-logic device is also prevented. A nitride barrier layer is intended on the upper main surface of a high-melting metal silicide film on a flat area formed by the upper side wall of a nitride film. When an elec. connection is made between the upper wiring and the **source/drain areas** by means of via **holes**, if the via **hole** positions are shifted, direct contact is avoided between the polycide gates and the contact **holes**. The threshold adjustment limit between the via **holes** and the gate electrode can be reduced in relation to the adjustment accuracy, which makes a redn. possible of the surfaces of the gate device components.

L38 ANSWER 2 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:731217 HCAPLUS
DN 135:265710
TI Integrated SRAM memory cell
IN Beer, Peter
PA Infineon Technologies A.-G., Germany
SO PCT Int. Appl., 30 pp.
CODEN: PIXXD2
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001073847	A1	20011004	WO 2001-EP3537	20010328
	W: JP, KR, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
	DE 10016444	A1	20011011	DE 2000-10016444	20000329
	DE 10016444	C2	20020124		
	EP 1181721	A1	20020227	EP 2001-917125	20010328
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
PRAI	DE 2000-10016444	A	20000329		
	WO 2001-EP3537	W	20010328		

AB The invention relates to an SRAM memory cell, comprising (a) a planar selection **MOSFET**; (b) a 1st and a 2nd N **channel**

MOSFET connected in series, arranged along a sidewall of a trough; (c) a 1st and a 2nd connected P **channel MOSFET**, arranged along a 2nd sidewall of the trough opposite the 1st side; (d) a 1st conducting layer arranged on the base of the trough, for the elec. connection of the **source** connector **region** of the 2nd N **channel MOSFET** and the 2nd P **channel MOSFET**; (e) a 2nd conducting layer which forms the gate connections for the 2nd N **channel MOSFET** and the 2nd P **channel MOSFET**; (f) a 3rd conducting layer which forms the gate connections of the 1st N **channel MOSFET** and the 1st P **channel MOSFET**; (g) a 4th conducting layer for the elec. connection of the **drain** connection regions of the 1st N **channel MOSFET** and the 2nd P **channel MOSFET** and (h) 2 contacts running perpendicular to the semi-conductor surface, whereby the 1st contact connects the 1st and 3rd conducting layer to each other and the 2nd contact connects the 2nd and 4th elec. layers to each other.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 3 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:645656 HCAPLUS
DN 135:203950
TI Method to fabricate a **MOSFET** using selective epitaxial growth to form lightly doped **source/drain regions**
IN Ang, Ting Cheong; Quek, Shyue Fong; Ong, Puay Ing; Loong, Sang Yee
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6284609	B1	20010904	US 1999-435437	19991122

AB A method is presented for fabricating a sub-quarter micron **MOSFET** device. A semiconductor substrate is provided. Isolation regions are formed in this substrate. An **oxide layer** is provided overlying both the substrate and the isolation regions. The **oxide layer** is patterned and etched exposing 2 regions of the substrate. A selective epitaxial growth (SEG) is performed with in situ doping covering the 2 exposed substrate regions formed during the previous step. The doped SEG regions will form the source and **drain** contact regions of the **MOSFET**. The **oxide layer** region between the 2 doped SEG regions is then patterned and etched away exposing the substrate. This is followed by a gate oxide formation and either a polysilicon or metal gate deposition. Planarization is then performed on the surface to facilitate interconnection later in the process and to form the final gate structure. Thermal energy provided from processing steps or from a rapid thermal anneal (RTA) allows the doping atoms in the SEG regions to diffuse into the substrate thereby forming the **active source/drain regions**. This method allows precise control of the doping profile in the **active source/drain region**. An inter-level dielec. is then deposited over the entire surface. Contact **holes** are then etched in the inter-level dielec. and metalization patterned to allow interconnection to the completed **MOSFET** device.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 4 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:241807 HCAPLUS
DN 134:246234
TI Eliminating buried contact **trench** in **MOSFET** devices having self-aligned silicide
IN Wu, Shye-Lin
PA Texas Instruments - Acer Incorporated, Taiwan
SO U.S., 11 pp., Cont.-in-part of U.S. Ser. No. 65,323.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6211556	B1	20010403	US 1999-323773	19990601
	US 6127706	A	20001003	US 1998-65323	19980423
PRAI	US 1998-65323	A2	19980423		

AB A **MOSFET** device with buried contact structure on a semiconductor substrate has the following major elements with their relative locations. A gate insulator is on a portion of the substrate and a gate electrode is on the gate insulator. A gate sidewall structure is located on side-walls of the gate electrode. Inside the substrate, a lightly doped **source/drain region** is under the gate sidewall structure, and a doped **source/drain region** is abutting the lightly doped **source/drain region** and located aside from a region under the gate sidewall structure. In addn., a doped buried contact region is also in the substrate next to the doped **source/drain region**. On the substrate, a Si connection is located on a portion of the doped buried contact region, and a shielding block is on the doped buried contact region covering only a region uncovered by the Si connection. Specifically, the shielding block includes dielec. side-walls and Si side-walls and the shielding block is formed right next to the **edge** of the Si connection.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 5 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:1256 HCAPLUS
DN 134:65037
TI A CMOS integrated circuit having vertical transistors and a process for fabricating same
IN Hergenrother, John Michael; Monroe, Donald Paul
PA Lucent Technologies Inc., USA
SO Eur. Pat. Appl., 27 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1063697	A1	20001227	EP 2000-304778	20000606
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001028399	A2	20010130	JP 2000-181209	20000616
PRAI	US 1999-335646	A	19990618		

AB A process for fabricating a CMOS integrated circuit with vertical

MOSFET devices is disclosed. In the process, .gtoreq.3 layers of material are formed sequentially on a semiconductor substrate. The 3 layers are arranged such that the 2nd layer is interposed between the 1st and 3rd layers. The 2nd layer is sacrificial, i.e., the layer is completely removed during subsequent processing. The thickness of the 2nd layer defines the phys. gate length of the vertical **MOSFET** devices. After the .gtoreq.3 layers of material are formed on the substrate, the resulting structure is selectively doped to form an n-type region and a p-type region in the structure. Windows or **trenches** are formed in the layers in both the n-type region and the p-type region. The windows terminate at the surface of the Si substrate in which one of either a **source** or **drain region** is formed. The windows or **trenches** are then filled with a semiconductor material. This semiconductor plug becomes the vertical **channel** of the transistor. Therefore the cryst. semiconductor plug is doped to form a source extension, a **drain** extension, and a **channel** region in the plug. Subsequent processing forms the other of a source or **drain** on top of the vertical **channel** and removes the sacrificial 2nd material layer. The removal of the sacrificial 2nd layer exposes a portion of the doped semiconductor plug. The device gate dielec. is then formed on the exposed portion of the doped semiconductor plug. The gate electrode is then deposited. The phys. gate length of the resulting device corresponds to the deposited thickness of the 2nd material layer.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 6-9

L38 ANSWER 6 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:1254 HCAPLUS
DN 134:65035
TI Process for fabricating vertical transistors
IN Hergenrother, John Michael; Monroe, Donald Paul; Weber, Gary Robert
PA Lucent Technologies Inc., USA
SO Eur. Pat. Appl., 21 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1063694	A1	20001227	EP 2000-304797	20000606
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6197641	B1	20010306	US 1999-335707	19990618
	JP 2001057427	A2	20010227	JP 2000-183545	20000619
PRAI	US 1999-335707	A	19990618		
	US 1998-143274	A1	19980828		

AB A process for fabricating a vertical **MOSFET** device for use in integrated circuits is disclosed. In the process, .gtoreq.3 layers of material are formed sequentially on a semiconductor substrate. The 3 layers are arranged such that the 2nd layer is interposed between the 1st and 3rd layers. The 2nd layer is sacrificial, i.e., the layer is completely removed during subsequent processing. The thickness of the 2nd layer defines the phys. gate length of the vertical **MOSFET**. In the process the 1st and 3rd layers have etch rates that are significantly lower than the etch rate of the 2nd layer in an etchant selected to remove

the 2nd layer. The top layer, which is either the 3rd or subsequent layer, is a stop layer for a subsequently performed mech. polishing step that is used to remove materials formed over the .gtoreq.4 layers. After the .gtoreq.3 layers of material are formed on the substrate, a window or **trench** is formed in the layers. The window terminates at the surface of the Si substrate in which one of either a **source** or **drain region** is formed in the Si substrate. The window or **trench** is then filled with a semiconductor material. This semiconductor plug becomes the vertical **channel** of the transistor. Therefore the cryst. semiconductor plug is doped to form a source extension, a **drain** extension, and a **channel** region in the plug. Subsequent processing forms the other of a source or **drain** on top of the vertical **channel** and removes the sacrificial 2nd material layer. The removal of the sacrificial 2nd layer exposes a portion of the doped semiconductor plug. The device gate dielec. is then formed on the exposed portion of the doped semiconductor plug. The gate electrode is then deposited. The phys. gate length of the resulting device corresponds to the deposited thickness of the 2nd material layer.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 7 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:900940 HCAPLUS
DN 134:64907
TI A method of manufacturing a semiconductor device with a transistor having a dielectric gate of shorter length
IN Stolk, Peter A.; Ponomarev, Youri
PA Koninklijke Philips Electronics N.V., Neth.
SO PCT Int. Appl., 25 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000077828	A2	20001221	WO 2000-EP5012	20000531
	WO 2000077828	A3	20010712		
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 1138058	A2	20011004	EP 2000-938722	20000531
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
PRAI	EP 1999-201869	A	19990611		
	WO 2000-EP5012	W	20000531		

AB In a method of manufg. a semiconductor device comprising a transistor having a gate insulated from a **channel** by a gate dielec., which **channel** is provided in an **active region** of a first cond. type provided at a surface of a semiconductor body and has a length L over which it extends between a **source zone** and a **drain** zone of a second cond. type, the **active region** of the first cond. type is defined in the semiconductor body, and a **dielec. layer** is applied which is provided with a recess at the area of the gate planned to be provided at a later stage, in which recess an **insulating layer** is applied, forming the gate dielec. of the transistor. A first conductive layer and a second conductive layer are applied, the first conductive layer being relatively thin compared to the width of the recess, which first

conductive layer and second conductive layer jointly form the gate of the transistor and fill the recess in the **dielec. layer**. The gate comprises a central portion and side end portions positioned along either side of the central portion, which central portion and side end portions are in contact with the gate dielec. and jointly establish a work function of the gate varying across the length L of the **channel**.

L38 ANSWER 8 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:769035 HCAPLUS
DN 133:316464
TI Method of making high performance **MOSFET** with integrated simultaneous formation of source/**drain** and gate regions
IN Gardner, Mark I.; Gilmer, Mark C.; Paiz, Robert
PA Advanced Micro Devices, Inc., USA
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6140191	A	20001031	US 1998-157973	19980921

AB An integrated circuit and a method of making a transistor thereof are provided. The method includes the steps of forming a 1st stack on the substrate and a 2nd stack on substrate in spaced-apart relation to the 1st stack, where the 1st stack has a 1st layer and 1st and 2nd spacers adjacent to the 1st layer and the 2nd stack has a 2nd layer and 3rd and 4th spacers adjacent to the 2nd layer. A gate **dielec. layer** is formed on the substrate between the 1st and 2nd stacks and a 1st conductor layer is formed on the gate **dielec. layer**. A 1st **source/drain region** is formed beneath the 1st conductor layer and a 2nd **source/drain region** is formed beneath the 2nd conductor layer. The 1st and 2nd layers are removed and a 1st contact is formed on the 1st **source/drain region** and a 2nd contact is formed on the 2nd **source/drain region**. The method integrates gate and **source/drain region** formation and provides for gate electrodes with work functions tailored for n-**channel** and p-**channel** devices.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 9 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:383837 HCAPLUS
DN 133:11091
TI **MOS** thin film transistor and method of fabricating same
IN Yamazaki, Shunpei; Ohtani, Hisashi; Suzawa, Hideomi; Takayama, Toru
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 66 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1006589	A2	20000607	EP 1999-124230	19991203
	EP 1006589	A3	20000927		

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,

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          IE, SI, LT, LV, FI, RO
     JP 2000228527     A2   20000815       JP 1999-345498   19991203
PRAI JP 1998-344746    A    19981203
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AB There is provided a cryst. TFT in which reliability comparable to or superior to a **MOS** transistor can be obtained and excellent characteristics can be obtained in both an on state and an off state. A gate electrode of the cryst. TFT is formed of a laminate structure of a 1st gate electrode made of a semiconductor material and a 2nd gate electrode made of a metal material. An n-**channel** TFT includes an LDD region, and a region overlapping with the gate electrode and a region not overlapping with the gate electrode are provided, so that a high elec. field in the vicinity of a **drain** is relieved, and at the same time, an increase of an off current is prevented.

=> D BIB AB 10-23

L38 ANSWER 10 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:367145 HCAPLUS
DN 132:355637
TI Semiconductor devices having a thin film field-effect transistor and corresponding manufacturing methods
IN Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 60 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

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     PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
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PI   EP 1005094         A2   20000531       EP 1999-123427   19991124
         R:  AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,
             IE, SI, LT, LV, FI, RO
     JP 2000223716      A2   20000811       JP 1999-334453   19991125
PRAI JP 1998-333623     A    19981125
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AB The gate electrode of a non-amorphous TFT consists of a 1st gate layer (113,116) disposed on a gate **insulating film** (103) and made of a material selected from Si, Ta, Ti, W or Mo and compds. thereof, a 2nd gate layer (114,117) disposed on said 1st gate layer at a distance from the **edge** of said 1st gate layer and made of a low resistivity material such as Cu or Al and a 3rd gate layer (115,118) disposed on said 1st and 2nd gate layers and made of a material selected from Si, Ta, Ti, W or Mo and compds. thereof, thereby to enhance the thermal resistance of the gate electrode. Besides, such an n-**channel** TFT may be provided with a low-concn. impurity region (106a,106b) which adjoins a **channel** region (104), and which includes a 1st subregion (106a) overlapped by the gate electrode and a 2nd subregion (106b) not overlapped by the gate electrode, thereby to mitigate a high elec. field near the **drain** (108) of the TFT and to simultaneously prevent the OFF current of the TFT from increasing.

L38 ANSWER 11 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:43921 HCAPLUS
DN 130:146987
TI Improving the characteristics of ultra-thin-**film** fully-depleted **metal-oxide-semiconductor** field effect transistors on SIMOX (separation by IMplanted OXygen) by selective tungsten deposition on **source** and **drain region**

AU Sato, Yasuhiro; Kosugi, Toshihiko; Tsuchiya, Toshiaki; Ishii, Hiromu
CS NTT Sysrenm Electronics Laboratories, Kanagawa, 243-0198, Japan
SO Jpn. J. Appl. Phys., Part 1 (1998), 37(12A), 6290-6294
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB Selective tungsten (W) chem.-vapor-deposition (CVD) with hydrogenation and hydrogen-termination (HHT) is applied to ultra-thin-film fully-depleted (FD) **metal-oxide-semiconductor** field effect transistors (**MOSFETs**) on SIMOX (Sepn. by IMplanted OXygen) for reducing the sheet resistance of **source** and **drain** **regions**. 0.25-.mu.m-gate **MOSFETs** on SIMOX (**MOSFETs**/SIMOX) with a top Si layer with a thickness of 50 nm are fabricated using selective W-CVD, and their characteristics, including hot-carrier effects and latch-onset voltage, are systematically investigated. It is found that selective W-CVD with HHT can reduce the source/**drain** (S/D) sheet resistance in 50-nm-thick ultra-thin-film SIMOX to 10 .OMEGA./sq. or less. This ensures that W deposition increases the **drain** satn. current. It is also found that W deposition largely suppresses the parasitic bipolar effects. Consequently, the anomalous subthreshold slope diminishes, hot carrier reliability improves, and the latch-onset voltage rises to over 2.5 V. Moreover, it is clarified that the parasitic bipolar effects are largely suppressed when the W layer is within 0.3 .mu.m from the source/body junction. This is because W effectively exts. the **holes** generated by impact ionization, and thus suppresses the accumulation of **holes** which would otherwise induce an increase in the body potential.
RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 12 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:140927 HCAPLUS
DN 126:165245
TI Field effect semiconductor devices and their manufacture
IN Kuroda, Hideaki
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 30 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08335701	A2	19961217	JP 1995-325148	19951120
	JP 3209064	B2	20010917		
PRAI	JP 1995-42411	A	19950207		
	JP 1995-107903	A	19950407		

AB The device has dummy patterns extending parallel to the gate electrode on the device isolation regions, insulating sidewalls formed on the sides of the gate electrodes and the dummy patterns, depressions between the sidewalls of the gate electrodes and those of the dummy patterns, and an elec. conductive layer in the depressions (e.g., sepd. from the gate electrodes by the sidewalls). The conductor layer requires no contact **hole** for connection to the diffusion layer, lowers the sheet resistance of the diffusion layer, can produce shallow **diffusion** **regions**, and requires contact plugs for connection to the overlying wiring **layer** through an interlayer **insulating**

film with increased allowance in alignment.

L38 ANSWER 13 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:612489 HCAPLUS
DN 125:236278
TI Semiconductor device with low contact resistance and its manufacture
IN Itsushiki, Kaihei; Watanabe, Hirobumi; Tanigawa, Tetsuo; Shindo, Yasuyuki
PA Ricoh Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08204009	A2	19960809	JP 1995-12436	19950130

AB The method involves the following steps: (1) in an **insulator film**, forming contact-**holes** which reach **source /drain regions**; (2) forming a high m.p. metal film on the bottoms of the contact-**holes**; (3) implanting Si ions into the high-m.p. metal film; and (4) thermally treating the whole to form silicide films at the bottoms of the contact-**holes**. In the step 4, not only the Si in the **source/drain regions** but also the Si implanted in the surface of the high-m.p. metal film diffuses towards the inside of the high-m.p. metal film, so that the silicide films are formed in a short time. A semiconductor device manufd. by the method is also claimed. The device is useful for **MOSFET**.

L38 ANSWER 14 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:548316 HCAPLUS
DN 125:183144
TI Manufacture of semiconductor memory devices
IN Takaishi, Yoshihiro
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08153857	A2	19960611	JP 1994-294394	19941129
	JP 2643870	B2	19970820		
	US 5726083	A	19980310	US 1995-562224	19951128
PRAI	JP 1994-294394		19941129		

AB The title process comprises (1) sequential formation of a N- and a P-well in regions for a part of the peripheral circuit, and the rest of the peripheral circuit and the memory array on a 1st cond. type Si substrate, a field **oxide** and gate **oxide film** on desired regions, and word lines and gate electrodes on regions of the memory array and the peripheral circuit, resp., a 1st n-diffusion layer on the p-well in the region of the memory array by ion implantation with a mask from the word lines and the field **oxide film**, and a 2nd n-diffusion layer on the p-well in the region of the peripheral circuit and a p-diffusion layer on the n-well by implantation of As ions and BF2 ions, resp., with a mask from the gate electrodes, the field **oxide film**, etc., (2) sequential formation of a 1st interlayer **insulating film** on the substrate surface and bit contact **holes** therethrough reaching the 1st n-diffusion layer, bit lines

being connected to the diffusion **layer**, a 2nd interlayer **insulating film** on the surface and storage node contact **holes** through the 1st and the 2nd interlayer **insulating film** reaching the 1st n-diffusion layer, storage node electrodes being connected to the 1st n-diffusion layer, and a Ta2O5 film covering the electrodes forming cell plate electrodes and the memory array, and a 3rd interlayer **insulating film** on the surface, (3) formation of 1st and 2nd contact **holes** reaching the n- and the p-diffusion layer, resp. Formation of a SiO2 protective film on the surface by plasma CVD, and implantation of P and BF2 ions in the 1st and the 2nd contact **holes** forming a n- and a p-ion implanted layer, resp., in shallow **regions** of the **diffusion** layers, (4) removal of the bottoms of the 1st and the 2nd contact **holes**, and the surface of the SiO2 film, sequential deposition of a Ti and a TiN film and silicidation thereof at 500f', CVD of a W film and etching back thereof leaving the film in the contact **holes**, sputtering deposition of an Al alloy film on the surface, and etching of the Al alloy, the TiN, and the Ti film forming a metal wiring for the peripheral circuit. A dynamic RAM having stacked capacitors and a peripheral circuit with complementary **MOS** devices may be produced, and increase of leakage current of the capacitor is suppressed and desired contact resistance is obtained.

L38 ANSWER 15 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:735300 HCAPLUS
DN 123:129646
TI **MOSFET**'s and manufacture thereof
IN Kimura, Shinichiro; Kure, Tokuo; Hisamoto, Masaru
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07038095	A2	19950207	JP 1993-182279	19930723

AB The title process comprises prepn. of a semiconductor substrate having low conc. **source-drain regions** and a 1st **insulating film** on its surface, sequential formation of an openings in the **insulating film**, **grooves** on the **channel** regions through the openings, gate **insulating film** in the **grooves**, and gate electrodes (e.g., from a refractory metal) on the 1st and the gate **insulating film**, removal of the 1st **insulating film** using the gate electrodes as a mask, formation of a side wall **insulating film** on the sides of the 1st **insulating film** and the gate electrodes in self-alignment, and doping to form high concn. **source-drain regions** using the side wall **insulating film** as a mask. Short **channel** effect is suppressed and gate-**drain** capacitance is made small with the thickness of the 1st **insulating film**.

L38 ANSWER 16 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:92498 HCAPLUS
DN 118:92498
TI Manufacture of **MOS** transistors
IN Saito, Shuichi

PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04192563	A2	19920710	JP 1990-324803	19901127

AB Manuf. of an **MOS** transistor includes (a) after prepg. a gate electrode or **source** and **drain regions**, forming a spacer from an oxide or nitride or metal film, or poly-Si; (b) forming an opening, with the use of a resist, in only the area corresponding to the **source region**; (c) implanting **channel**-forming impurity ions (e.g., B) through the opening; and (d) thermally activating the impurity. The method can decrease practical **channel** length.

L38 ANSWER 17 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:141973 HCAPLUS
DN 116:141973
TI Semiconductor-on-insulator **MOS** transistor and its manufacture
IN Yamano, Takeshi; Yamaguchi, Yasuo; Ajika, Natsuo
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03261178	A2	19911121	JP 1990-59680	19900310

AB A semiconductor-on-insulator **MOS** transistor comprises a high-m.p. metal **film** between a gate **insulating film** and **source-drain regions** under a gate electrode, and can prevent the charge-up in a **channel** region by flowing the charges generated in the **channel region** into the **source region**. A method for manufg. the transistor is also claimed.

L38 ANSWER 18 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:581880 HCAPLUS
DN 109:181880
TI Method for manufacturing a complementary **MOS** type semiconductor device
IN Sato, Masaki; Shinada, Kazuyoshi
PA Toshiba Corp., Japan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4743564	A	19880510	US 1985-813142	19851224
	JP 02048146	B4	19901024	JP 1985-164612	19850725
PRAI	JP 1984-276138		19841228		
	JP 1985-164612		19850725		

AB The method includes the following steps. A 1st and 2nd conductive

diffusion region are formed in a well region and a semiconductor substrate, resp., and a gate electrode is formed thereon. An **insulation layer** is formed on the semiconductor substrate and the well region. A contact **hole** is opened by selectively removing the **insulation layer** corresponding to the 1st and the 2nd conductive **diffusion regions**. At least 1 metal layer selected from a group consisting of metal (e.g., W) and metal (e.g., W) silicide having a high m.p. is formed on an exposed surface of the 1st and the 2nd conductive **diffusion regions**. The semiconductor substrate is heated to melt at least part of the **insulation layer** and form a tapered portion. A wiring layer is formed on the contact **hole**. This method prevents the contact resistance from increasing, the impurity of 1 region from diffusing into the other impurity regions, the impurity of the impurity regions from decreasing, and improves the reliability of the wiring layer by forming a tapered contact **hole**. These advantages permit high component d. by miniaturizing the device.

L38 ANSWER 19 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:178481 HCAPLUS
DN 108:178481
TI Preparation of buried **oxide layers** and **MOS** transistors
IN Kamins, Theodore I.; Colinge, Jean Pierre; Marcoux, Paul J.; Roylance, Lynn M.; Moll, John L.
PA Hewlett-Packard Co., USA
SO Ger. Offen., 12 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 3726842	A1	19880218	DE 1987-3726842	19870812
	US 4810664	A	19890307	US 1986-896560	19860814
PRAI	US 1986-896560		19860814		

AB Buried **oxide layers** are formed only under the **source** and **drain regions** by O ion implantation through a W- or nitride-contg. mask. The advantages of the Si-on-insulator structure (e.g., decreased capacitance and leakage current and increased speed) are retained, while the **channel** is coupled with the substrate and is kept at the same potential.

L38 ANSWER 20 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:141681 HCAPLUS
DN 108:141681
TI Manufacturing a **MOS** semiconductor device with a planarized conductive layer
IN Hiruta, Yoichi
PA Toshiba Corp., Japan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4713356	A	19871215	US 1986-833594	19860227

JP 61198780	A2	19860903	JP 1985-39235	19850228

PRAI JP 1985-39235 19850228

AB A method of manufg. a semiconductor device is described in which the proportion of the area occupied by the **source** and **drain** **regions** can be reduced. In this method, the side walls of a gate electrode are 1st selectively deposited with an **insulating** **film**, then conductive **material** layers are selectively formed on the **source** and **drain regions**, partially extending to side portions of element isolation regions, and, after forming an **insulating** protective **film** over the entire surface of the resultant structure, contact **holes** are formed to reach the conductive material layers for forming source and **drain** wiring layers.

L38 ANSWER 21 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:506860 HCAPLUS
DN 105:106860
TI Gate, contact, and interconnection structures of an **MOS** integrated circuit
PA Texas Instruments Inc., USA
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61081668	A2	19860425	JP 1985-137653	19850624
	JP 05077175	B4	19931026		
	US 4874720	A	19891017	US 1987-136043	19871221

PRAI US 1984-624166 19840625

AB The gate, contact, and interconnection structures of an **MOS** integrated circuit consists of: (1) a W electrode formed on a Si substrate via a Si **oxide** thin **layer**; (2) an **oxide** **coating**, which encapsulates the gate electrode, on the side walls of the gate electrode; (3) highly doped **source-drain** **regions** self-aligned with the side-wall coating; (4) a W layer, which is self-aligned with the side-wall coating, on the **source-drain regions**; (5) a thick **insulator** **coating** on the gate electrode, W layer, and **source-drain regions**; and (6) metal contacts contacting the silicide layer via the contact **holes** in the **insulator** **coating** and an interconnection strip consisting of successive layers of Mo, W, and Au. A method for the prepn. of the structures are also described.

L38 ANSWER 22 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:506853 HCAPLUS
DN 105:106853
TI Gate, contact, and interconnection structure of an **MOS** integrated circuit
PA Texas Instruments Inc., USA
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 61081670 A2 19860425 JP 1985-137655 19850624
JP 05081052 B4 19931111
PRAI US 1984-624165 19840625

AB The gate, contact, and interconnection structures of an **MOS** integrated circuit consists of the following: (1) a metal gate of a thin Mo layer on a SiO_2 thin layer, a relatively thick W layer on the Mo **layer**, and an **oxide coating** on the gate and gate side walls; (2) highly doped **source-drain regions** self-aligned with side-wall **oxide coating**; (3) a W silicide layer self-aligned with the side-wall **oxide coating** on the **source-drain regions**; (4) a thick **insulator coating** on the gate, W silicide layer and **source-drain regions**; and (5) metal contacts and interconnection strips contacting the W silicide layer via contact **holes** in the **insulator coating**. Addnl., the metal contacts and interconnection strips consist of a thin W layer only in the contact **holes**, a thin Mo layer on the W **layer** and **insulator coating**, a relatively thick W layer on the Mo layer, and a Au layer on the relatively thick W layer.

L38 ANSWER 23 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:452865 HCAPLUS
DN 105:52865
TI Patterned implanted buried-oxide transistor structures
AU Kamins, T. I.; Marcoux, P. J.; Moll, J. L.; Roylance, L. M.
CS Hewlett-Packard Lab., Palo Alto, CA, 94304, USA
SO J. Appl. Phys. (1986), 60(1), 423-6
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English

AB **MOSFET**'s were fabricated with a buried-**oxide layer** implanted under only the **source** and **drain regions**. W selectively chem. vapor deposited over the polysilicon gate electrode limited the O-implanted area and provided a self-aligned structure. The surface of the **source** and **drain regions** was raised above that of the **channel** by the implanted oxide. The buried oxide formed under the **source** and **drain regions** joined smoothly with the surrounding field oxide. Some addnl. oxide was formed beneath the thermally grown field oxide by the implanted O, and significant field oxide was apparently removed by sputtering during the implantation. A simplified, non-optimum, transistor-fabrication process produced depletion-mode, n-**channel** devices which exhibited transistor action.